	L #	Hits	Search Text	DBs
1	L1	9161	instruction near10 (valid$3 invalid$3 correct incorrect)	USPAT; US-PGPUB
2	L4	418	(instruction near10 (valid$3 invalid$3 correct incorrect)).ab,ti.	USPAT; US-PGPUB
3	L6	34856	instruction near10 (select$3 replac$5 substitut$3)	USPAT; US-PGPUB
4	L7	694	1 near99 6	USPAT; US-PGPUB
5	L8	87	7 and 4	USPAT; US-PGPUB
6	L9	2570	instruction near10 (valid$3 invalid$3 correct incorrect)	EPO; JPO; DERWENT; IBM_TDB
7	L10	13056	instruction near10 (select$3 replac$5 substitut$3)	EPO; JPO; DERWENT; IBM_TDB
8	L11	123	9 near99 10	EPO; JPO; DERWENT; IBM_TDB
9	L17	38060	instruction near10 (predetermind speci$4 valid$3 invalid$3 correct incorrect)	USPAT; US-PGPUB
10	L18	2869	(instruction near10 (predetermined speci$4 valid$3 invalid$3 correct incorrect)).ab,ti.	USPAT; US-PGPUB
11	L20	11026	instruction near10 (predetermind speci$4 valid$3 invalid$3 correct incorrect)	EPO; JPO; DERWENT; IBM_TDB
12	L21	595	20 near99 10 not 11	EPO; JPO; DERWENT; IBM_TDB
13	L19	23	4 near99 17 and 18 not 8	USPAT; US-PGPUB
14	L26	4378	17 near20 (select$3 replac$5 substitut$3) not (8 19)	USPAT; US-PGPUB
15	L27	3836	17 near10 (select$3 replac$5 substitut$3) not (8 19)	USPAT; US-PGPUB
16	L28	131	20 near20 (select23 replac$5 substitut$3) not 11	EPO; JPO; DERWENT; IBM_TDB

	Document ID	U	Title	Current OR
1	US 20030188124 A1	☐	History-based carry predictor for data cache address generation	711/214
2	US 20030182540 A1	☒	Method for limiting physical resource usage in a virtual tag allocation environment of a microprocessor	712/225
3	US 20030182537 A1	☒	Mechanism to assign more logical load/store tags than available physical registers in a microprocessor system	712/216
4	US 20030120898 A1	☒	Method and circuits for early detection of a full queue	712/205
5	US 20030105943 A1	☒	Mechanism for processing speclative LL and SC instructions in a pipelined processor	712/216
6	US 20030093781 A1	☒	Method and apparatus for linking converted applet files without relocation annotations	717/162
7	US 20030056088 A1	☒	Processor, compiler and compilation method	712/214
8	US 20030037225 A1	☒	Apparatus and method for microcontroller debugging	712/227
9	US 20030033505 A1	☒	Apparatus for processing instructions in a computing system	712/215
10	US 20030014473 A1	☒	Multi-thread executing method and parallel processing system	709/107
11	US 20020194462 A1	☒	Apparatus and method for selecting one of multiple target addresses stored in a speculative branch target address cache per instruction cache line	712/238
12	US 20020194460 A1	☒	Apparatus, system and method for detecting and correcting erroneous speculative branch target address cache branches	712/238
13	US 20020156997 A1	☒	Method for mapping instructions using a set of valid and invalid logical to physical register assignments indicated by bits of a valid vector together with a logical register list	712/217
14	US 20020083312 A1	☒	Branch Prediction apparatus and process for restoring replaced branch history for use in future branch predictions for an executing program	712/240
15	US 20020069346 A1	☒	METHOD FOR MAPPING INSTRUCTIONS USING A SET OF VALID AND INVALID LOGICAL TO PHYSICAL REGISTER ASSIGNMENTS INDICATED BY BITS OF A VALID VECTOR TOGETHER WITH A LOGICAL REGISTER LIST	712/216
16	US 20020040426 A1	☒	Execution control apparatus of data driven information processor	712/25
17	US 20020013691 A1	☒	Method and apparatus for processor code optimization using code compression	703/22

	Document ID	U	Title	Current OR
18	US 20010 02026 7 A1	☒	Pipeline processing apparatus with improved efficiency of branch prediction, and method therefor	712/239
19	US 20010 01687 0 A1	☒	Method for at least making ready for mailing at least one message, and data structure for use therein	709/203
20	US 65429 87 B1	☒	Method and circuits for early detection of a full queue	712/217
21	US 65264 96 B1	☒	Burst instruction alignment method apparatus and method therefor	711/201
22	US 65264 81 B1	☒	Adaptive cache coherence protocols	711/147
23	US 64776 40 B1	☒	Apparatus and method for predicting multiple branches and performing out-of-order branch resolution	712/238
24	US 64053 04 B1	☒	Method for mapping instructions using a set of valid and invalid logical to physical register assignments indicated by bits of a valid vector together with a logical register list	712/216
25	US 63851 86 B1	☒	Down-traffic-signal transmission system	370/342
26	US 62533 74 B1	☒	Method for validating a signed program prior to execution time or an unsigned program at execution time	717/126
27	US 62470 97 B1	☒	Aligned instruction cache handling of instruction fetches across multiple predicted branch instructions	711/125
28	US 62021 42 B1	☒	Microcode scan unit for scanning microcode instructions using predecode data	712/204
29	US 61700 82 B1	☒	Taking corrective action in computer programs during instruction processing	717/127
30	US 61674 60 A	☒	System for replacing control information in a printer according to external instruction information if a replacement function is valid	710/5
31	US 61579 98 A	☒	Method for performing branch prediction and resolution of two or more branch instructions within two or more branch prediction buffers	712/238
32	US 61482 92 A	☒	Method for statistics mode reloading and for statistical acquisition according to statistics classes in the storing of a dataset	705/30
33	US 60980 59 A	☒	Computer implemented machine learning method and system	706/13
34	US 60790 06 A	☒	Stride-based data address prediction structure	711/213
35	US 60598 40 A	☒	Automatic scheduling of instructions to reduce code size	717/154
36	US 59681 69 A	☒	Superscalar microprocessor stack structure for judging validity of predicted subroutine return addresses	712/239
37	US 59681 63 A	☒	Microcode scan unit for scanning microcode instructions using predecode data	712/204
38	US 59648 62 A	☒	Execution unit and method for using architectural and working register files to reduce operand bypasses	712/23
39	US 59616 36 A	☒	Checkpoint table for selective instruction flushing in a speculative execution unit	712/228

	Document ID	U	Title	Current OR
40	US 5920890 A	☒	Distributed tag cache memory system and method for storing data in the same	711/144
41	US 5887185 A	☒	Interface for coupling a floating point unit to a reorder buffer	712/23
42	US 5875315 A	☒	Parallel and scalable instruction scanning unit	712/204
43	US 5872947 A	☒	Instruction classification circuit configured to classify instructions into a plurality of instruction types prior to decoding said instructions	712/213
44	US 5870575 A	☒	Indirect unconditional branches in data processing system emulation mode	712/209
45	US 5859991 A	☒	Parallel and scalable method for identifying valid instructions and a superscalar microprocessor including an instruction scanning unit employing the method	712/204
46	US 5854921 A	☒	Stride-based data address prediction structure	712/239
47	US 5852727 A	☒	Instruction scanning unit for locating instructions via parallel scanning of start and end byte information	712/215
48	US 5850630 A	☒	Tool kit with audible prompting for first aid and the like	704/270
49	US 5850532 A	☒	Invalid instruction scan unit for detecting invalid predecode data corresponding to instructions being fetched	712/213
50	US 5841947 A	☒	Computer implemented machine learning method and system	706/13
51	US 5809271 A	☒	Method and apparatus for changing flow of control in a processor	712/208
52	US 5796970 A	☒	Information processing apparatus for realizing data transfer for a plurality of registers using instructions of short word length	712/200
53	US 5790826 A	☒	Reduced register-dependency checking for paired-instruction dispatch in a superscalar processor with partial register writes	712/216
54	US 5757690 A	☒	Embedded ROM with RAM valid bits for fetching ROM-code updates from external memory	365/104
55	US 5742785 A	☒	Posting multiple reservations with a conditional store atomic operations in a multiprocessing environment	712/217
56	US 5737749 A	☒	Method and system for dynamically sharing cache capacity in a microprocessor	711/123
57	US 5729728 A	☒	Method and apparatus for predicting, clearing and redirecting unpredicted changes in instruction flow in a microprocessor	712/234
58	US 5717587 A	☒	Method and system for recording noneffective instructions within a data processing system	700/2
59	US 5692153 A	☒	Method and system for verifying execution order within a multiprocessor data processing system	711/141
60	US 5687338 A	☒	Method and apparatus for maintaining a macro instruction for refetching in a pipelined processor	712/205
61	US 5687336 A	☒	Stack push/pop tracking and pairing in a pipelined processor	712/202
62	US 5682206 A	☒	Consumer interface for programming device	725/58

	Document ID	U	Title	Current OR
63	US 5649137 A	☒	Method and apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency	712/207
64	US 5619408 A	☒	Method and system for recoding noneffective instructions within a data processing system	712/226
65	US 5596733 A	☒	System for exception recovery using a conditional substitution instruction which inserts a replacement result in the destination of the excepting instruction	712/244
66	US 5581774 A	☒	Data processor decoding and executing a train of instructions of variable length at increased speed	712/210
67	US 5522084 A	☒	Method and system for invalidating instructions utilizing validity and write delay flags in parallel processing apparatus	712/23
68	US 5511175 A	☒	Method an apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency	712/216
69	US 5500942 A	☒	Method of indicating parallel execution compoundability of scalar instructions based on analysis of presumed instructions	712/210
70	US 5479616 A	☒	Exception handling for prefetched instruction bytes using valid bits to identify instructions that will cause an exception	712/212
71	US 5438670 A	☒	Method of prechecking the validity of a write access request	711/3
72	US 5437017 A	☒	Method and system for maintaining translation lookaside buffer coherency in a multiprocessor data processing system	709/213
73	US 5420990 A	☒	Mechanism for enforcing the correct order of instruction execution	712/216
74	US 5418917 A	☒	Method and apparatus for controlling conditional branch instructions for a pipeline type data processing apparatus	712/234
75	US 5414822 A	☒	Method and apparatus for branch prediction using branch prediction table with improved branch prediction effectiveness	712/240
76	US 5243705 A	☒	System for rapid return of exceptional processing during sequence operation instruction execution	712/228
77	US 5226130 A	☒	Method and apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency	712/238
78	US 5031096 A	☒	Method and apparatus for compressing the execution time of an instruction stream executing in a pipelined processor	711/169
79	US 5000446 A	☒	Color-coded weight stack pin system for exercise machines	482/101
80	US 4894772 A	☒	Method and apparatus for qualifying branch cache entries	712/240
81	US 4800563 A	☒	Error processing method and apparatus for information processing system	714/6
82	US 4791557 A	☒	Apparatus and method for monitoring and controlling the prefetching of instructions by an information processing system	712/244
83	US 4763255 A	☒	Method for generating short form instructions in an optimizing compiler	717/153
84	US 4617625 A	☒	Vector processor	712/4
85	US 4368534 A	☒	Keyboard controlled vital digital communication system	714/807

	Document ID	U	Title	Current OR
86	US 4323249 A	☒	Board game apparatus	273/249
87	US 3987420 A	☐	Electronic computer with equipment for debugging operative programs	717/131

	Document ID	U	Title	Current OR
1	US 20030 07460 1 A1	☐	Method of correcting a machine check error	714/15
2	US 20020 17428 0 A1	☒	Method of downloading application programs on the editing system platform of an electronic communication apparatus	710/260
3	US 64497 09 B1	☒	Fast stack save and restore system and method	712/202
4	US 62436 20 B1	☒	Computerized manual mail distribution method and apparatus with feeder belt system	700/223
5	US 61784 84 B1	☒	DCBST with ICBI mechanism to maintain coherency of bifurcated data and instruction caches	711/145
6	US 61674 71 A	☒	Method of and apparatus for dispatching a processing element to a program location based on channel number of received data	710/62
7	US 61015 82 A	☒	Dcbst with icbi mechanism	711/141
8	US 59745 36 A	☒	Method, system and computer program product for profiling thread virtual memory accesses	712/215
9	US 59616 33 A	☒	Execution of data processing instructions	712/216
10	US 59319 57 A	☒	Support for out-of-order execution of loads and stores in a processor	714/48
11	US 57614 74 A	☒	Operand dependency tracking system and method for a processor that executes instructions out of order	712/217
12	US 57489 34 A	☒	Operand dependency tracking system and method for a processor that executes instructions out of order and that permits multiple precision data words	712/216
13	US 57404 42 A	☒	Method and apparatus for identifying and correcting date calculation errors caused by truncated year values	717/124
14	US 57297 23 A	☒	Data processing unit	712/222
15	US 56869 20 A	☒	Transponder maintenance mode method	342/42
16	US 56196 71 A	☒	Method and apparatus for providing token controlled access to protected pages of memory	711/202
17	US 55817 21 A	☒	Data processing unit which can access more registers than the registers indicated by the register fields in an instruction	712/200
18	US 54500 87 A	☒	Transponder maintenance mode method	342/42
19	US 50458 44 A	☒	Image paralleling and rotating system	345/652
20	US 48538 49 A	☒	Multi-tasking register set mapping system which changes a register set pointer block bit during access instruction	711/202
21	US 47574 45 A	☒	Method and apparatus for validating prefetched instruction	712/207
22	US 47108 66 A	☒	Method and apparatus for validating prefetched instruction	712/207

	Document ID	U	Title	Current OR
23	US 4373179 A	☐	Dynamic address translation system	711/207

	Document ID	U	Title	Current OR
1	JP 2003029985 A	☐	MULTITHREAD EXECUTION METHOD AND PARALLEL PROCESSOR SYSTEM	
2	JP 2002352108 A	☒	PROXY MAIL TRANSMISSION SYSTEM, PROXY REPRESENTATIVE TRANSMITTING MAIL, MAIL PROXY TRANSMISSION METHOD AND PROCESSING PROGRAM THEREOF	
3	JP 2002314519 A	☒	BIT SYNCHRONIZING CIRCUIT	
4	JP 2001184209 A	☒	DEVICE AND METHOD FOR DECODING INSTRUCTION CODE	
5	JP 2001034471 A	☒	VLIW SYSTEM PROCESSOR	
6	JP 2001022582 A	☒	MICROPROCESSOR OF LOW POWER CONSUMPTION AND MICROPROCESSOR SYSTEM	
7	JP 2000315096 A	☒	MAN-MACHINE SYSTEM PROVIDED WITH VOICE RECOGNITION DEVICE	
8	JP 2002098587 A	☒	PROCESSOR HAVING DEVICE BRANCHED TO SPECIFIED PARTY DURING INSTRUCTION REPETITION	
9	JP 2002016823 A	☒	MULTIPLEX SYSTEM	
10	JP 2001012753 A	☒	METHOD FOR CONTROLLING MILLI-MODE BY BRANCH HISTORY TABLE DISABLE	
11	JP 11332470 A	☒	FROZEN DESSERT FEED SYSTEM	
12	JP 11149372 A	☒	FORCED PAGE ZERO PAGING SYSTEM FOR MICRO CONTROLLER USING DATA RAM	
13	JP 11136379 A	☒	INFORMATION PROCESSING METHOD, INFORMATION PROCESSING UNIT AND COMPUTER-READABLE STORAGE MEDIUM THEREOF	
14	JP 11102414 A	☒	METHOD AND DEVICE FOR CORRECTING OPTICAL CHARACTER RECOGNITION BY USING BITMAP SELECTION AND COMPUTER-READABLE RECORD MEDIUM RECORD WITH SERIES OF INSTRUCTIONS TO CORRECT OCR OUTPUT ERROR	
15	JP 10254971 A	☒	DATA PROCESSING DEVICE AND METHOD, AND STORAGE MEDIUM STORING COMPUTER READABLE PROGRAM	
16	JP 09200224 A	☒	NO-HIT SWITCHING METHOD	
17	JP 09152904 A	☒	PROGRAMMABLE CONTROLLER	
18	JP 08137687 A	☒	PROGRAM CONTROLLER	
19	JP 08129874 A	☒	FIFO MEMORY	

	Document ID	U	Title	Current OR
20	JP 07281 894 A	☒	METHOD TO OPERATE PROCESSING SYSTEM AND PROCESSING SYSTEM	
21	JP 06284 163 A	☒	DATA SELECT CIRCUIT	
22	JP 06195 519 A	☒	DEVICE AND METHOD FOR CHARACTER RECOGNITION	
23	JP 06161 954 A	☒	DATA WIDTH CONVERTING BUFFER DEVICE	
24	JP 06120 855 A	☒	AUTOMATIC SIGNAL SWITCHING METHOD	
25	JP 06089 174 A	☒	COMPUTER MEMORY SYSTEM	
26	JP 06067 877 A	☒	INSTRUCTION FETCHING CIRCUIT	
27	JP 05342 105 A	☒	CACHE INVALIDATION PROCESSOR	
28	JP 05298 050 A	☒	MENU MISOPERATION CORRECTING DEVICE	
29	JP 05241 821 A	☒	DATA PROCESSOR	
30	JP 05241 820 A	☒	MICROPROGRAM CONTROLLER	
31	JP 05165 541 A	☒	ELECTRONIC CIRCUIT	
32	JP 05150 972 A	☒	PROGRAM CORRECTING SYSTEM	
33	JP 05135 032 A	☒	DOCUMENT PROCESSING METHOD	
34	JP 05127 720 A	☒	OFFLINE INSTRUCTION DEVICE FOR ROBOT	
35	JP 05035 175 A	☒	EDUCATIONAL SYSTEM	
36	JP 05020 188 A	☒	CACHE CONTROLLER	
37	JP 04338 825 A	☒	ARITHMETIC PROCESSOR	
38	JP 04283 856 A	☒	DOCUMENT PROCESSOR	
39	JP 04074 227 A	☒	OPTIMIZATION SYSTEM FOR MACHINE WORD CODE	
40	JP 04058 329 A	☒	ARITHMETIC PROCESSOR	
41	JP 03269 728 A	☒	INSTRUCTION EXECUTION CONTROL SYSTEM FOR PIPELINE COMPUTER	
42	JP 03148 731 A	☒	SINGLE CHIP MICROCOMPUTER	

	Document ID	U	Title	Current OR
43	JP 02238 530 A	☒	TEST SYSTEM FOR WORKING OF PROGRAM	
44	JP 02208 728 A	☒	VIRTUAL INSTRUCTION CACHE RE-REPLENISHMENT ALGORITHM	
45	JP 02137 489 A	☒	IMAGE ENCODING TRANSMISSION EQUIPMENT INCLUDING MOTION COMPENSATION	
46	JP 02123 440 A	☒	BUFFER STORAGE DEVICE	
47	JP 02068 622 A	☒	PROGRAM SPECIALIZING SYSTEM	
48	JP 02067 677 A	☒	LOW LEVEL CODE MAINTENANCE SYSTEM	
49	JP 02032 424 A	☒	INSTRUCTION PROCESSOR	
50	JP 01149 144 A	☒	AUTOMATIC FORMING SYSTEM FOR TEST DATA	
51	JP 01142 830 A	☒	MICROPROGRAM PROVIDED WITH EXPANDING/BRANCHING FUNCTION	
52	JP 01123 320 A	☒	METHOD AND DEVICE FOR FORMING SEARCH COMMAND	
53	JP 01044 524 A	☒	DATA PROCESSING SYSTEM	
54	JP 01031 671 A	☒	RECORDER	
55	JP 63254 834 A	☒	AUTOMOBILE TELEPHONE SET	
56	JP 63217 424 A	☒	INFORMATION PROCESSOR FOR PIPELINE CONTROL	
57	JP 63171 063 A	☒	IMAGE PROCESSOR	
58	JP 63098 788 A	☒	RECOGNIZING DEVICE	
59	JP 63093 065 A	☒	CONVERTING SYSTEM FOR COPROCESSOR ID	
60	JP 62176 335 A	☒	SIGNAL INTENSITY INDICATOR FOR RECEIVER	
61	JP 62159 233 A	☒	INSTRUCTION PREFETCHING DEVICE	
62	JP 62118 443 A	☒	METHOD OF AVOIDING STORAGE FAULT IN INFORMATION PROCESSING DEVICE	
63	JP 61138 356 A	☒	ONE-CHIP MICROCONTROLLER	
64	JP 57209 547 A	☒	COLLECTING DEVICE FOR PROGRAM EXECUTING CARRIER INFORMATION	
65	JP 57016 320 A	☒	DATE SETTING DEVICE FOR ELECTRONIC BALANCE PROVIDED WITH LABEL ISSUING FUNCTION	

	Document ID	U	Title	Current OR
66	JP 56033 742 A	☒	ARITHMETIC PROCESSOR HAVING DEBUG PROCESSING FUNCTION	
67	EP 88960 8 A2	☒	Down-traffic-signal transmission system	
68	EP 76490 0 A2	☒	Information processing apparatus for realizing data transfer to/from a plurality of registers using instructions of short word length	
69	EP 71636 4 A1	☒	Operator support system	
70	GB 22851 55 A	☒	System for exception recovery using a conditional sbstitution instruction which inserts a replacement result in the destination of the excepting instruction	
71	EP 23902 3 A1	☒	Arrangement for processing branch instructions in pipelined data-processing systems.	
72	US 20030 09378 1 A	☒	Instruction boundaries determining method for smart cards, involves examining instructions selected from instruction group and terminating instructions beyond pointer that detects instruction related to method body	
73	US 20030 10594 3 A	☒	Processor for multiprocessing system, has fetch/decode/issue unit to reject speculative load linked instruction for issue, when valid reservation indication is received from batch prediction unit	
74	US 65464 78 B	☒	Processor locates specific instruction in response to fetch address, when each instruction pointer within selected initial entry corresponding to fetch address, is valid	
75	JP 20031 86663 A	☒	Data processing system determines content to be corrected based on content transfer instructions and compares corrected content with selected data so as to notify correction completion state	
76	US 64635 24 B	☒	Multiple store instructions issuing method in superscalar data processing system, involves issuing selected address and data operands in single queue instruction slot to load/store and fixed point units, for execution	
77	JP 20022 78744 A	☒	Printer system corrects printing data using setting value selected based on instructions received from user	
78	US 64571 23 B	☒	System change file generation method in computer system, involves selecting instruction module for correcting indicated problems	
79	DE 10035 642 C	☒	Laundry machine has program control provided with display device for clear text display of operating programs and program parameters	
80	US 62725 61 B	☒	Sound blaster interface card auto-detection method, involves identifying detection of card to be successfully completed on receiving an interruption	
81	JP 20010 22611 A	☒	Program conversion procedure for computer system, involves recognizing validity of output instructions extracted from source program and accordingly program is converted to invalidate other instructions	
82	JP 20010 15690 A	☒	Large scale integrated system outputs initialization information corresponding to address value output by CPU to internal data bus, when selecting signal is invalid	
83	US 61759 41 B	☒	Error correcting code error correction apparatus, has sequencer that is selectably operable to cause application of instructions to finite field arithmetic logic unit and integer arithmetic logic unit	
84	JP 20003 47862 A	☒	Instruction changing circuit for single-chip microcomputer has selector provided in ROM collection unit having flag of operation which shows implication of selection of correction instruction	

	Document ID	U	Title	Current OR
85	JP 2000267721 A	☒	Operation menu controller of supervision and control system, has modification unit for displaying main operation menu to rectify operation error which is identified during execution of selected operation menu	
86	GB 2345362 A	☒	Information processing system in which three processors constructing multiplex unit are connected by bus has invalidating unit for changing value in instructing register to another value when new processor replaces faulty unit	
87	GB 2345354 A	☒	Method of sound card interface auto detection	
88	JP 2000172504 A	☒	Instruction fetching method for microprocessor involves holding selective portion of instruction corresponding to branch established by instruction praxis in processor	
89	CN 1254135 A	☒	Writing aid system and its method	
90	EP 889608 A	☒	Down traffic signal transmission system e.g. for mobile communication system - has communication between base stations and mobile station performed in accordance with CDMA scheme with spread coding apparatus provided in base station having valid signal determination unit to determine control signal in received signal	
91	US 5835583 A	☒	Call processing method for information service providers - involves processing first response from database of selected information service provider to validate call processing instruction	
92	JP 10224147 A	☒	Frequency adjusting device for oscillation circuit - stores correction data for oscillation frequency adjustment, which is read based on program instruction, according to which any one of capacitors for frequency adjustment is selected	
93	US 5758143 A	☒	Updating method for branch history table in data processor such as computer - involves selecting data corresponding to two main instructions for modification of BHT, based on validity of branch path formation judgment result	
94	EP 843245 A	☒	Positioning method for geo-stationary satellite swarm - involves selecting one satellite as master satellite in contact with ground station, which provides position correction instructions, and causing correction instructions to be executed simultaneously by remaining satellites of swarm	
95	US 5748978 A	☒	Instruction selection and alignment appts for microprocessor - has control unit that shifts second valid indication into first valid indication if first instruction is selected and shifts second portion of queue into first portion of queue if instructions in first portion of queue have been dispatch	
96	US 5742794 A	☒	Computer apparatus with emulation circuitry - which replaces invalid instructions with code which can be interpreted by processor sub-system	
97	US 5717587 A	☒	Method of recording non-effective instruction in data processing system - involves re-coding selected instruction into specified instruction format prior to further processing of selected instruction	
98	EP 796012 A	☒	Television signal recording and=or reproducing apparatus - has device which selectively instruct whether resolution reinforcement signal in television signal portion is validated or not, and generates selection signal	
99	JP 09189204 A	☒	Steam turbine controller for electric power generation plant - includes selection unit which selects correction operating instruction corresponding to steam governing valves and main stop valve	
100	US 5619408 A	☒	Instruction processing method for data processing system of superscalar, pipelined microprocessor - involves determining if selected instruction would be noneffective if executed by processor, and dispatching it to completion buffer if it does or recoding selected instruction, prior to dispatch to execution unit, if it does not	

	Document ID	U	Title	Current OR
101	GB 2300496 A	☒	Data processing system with program error correction - includes processor executing instructions and providing related output data for storage in history memory with controller selecting different memory on error detection	
102	JP 08185319 A	☒	Program correction method for microcomputer - involves using selector to output unconditional branch instruction to program memory in response to coincidence signal received from equivalence circuit	
103	EP 716364 A	☒	Operator running support system for large scale e.g. nuclear, thermal or hydraulic power plant - compares guidance data operation instructions with selected output operation instructions to evaluate their correctness, with selected operation instructions being sent as control output when correct	
104	US 5479616 A	☒	Exception handling system for prefetched instruction bytes in pipelined 486-type microprocessor - stores prefetched instruction byte in queue with valid bit if byte is invalid, when exception occurs, and detects if stall condition results from exception associated with prefetched instruction byte by checking stored instruction status	
105	US 5420990 A	☒	Correct order instruction execution enforcement appts - uses CAM for storing load addresses of data read from memory by selected instructions, comparing store addresses with load addresses of data to be written to memory and generating signal, if load address is identical to compared store addre	
106	JP 07133092 A	☒	Misoperation prevention mechanism for construction machine e.g. cranes or shovels - incorporates operation control unit which obstructs movement of actuator from misoperating	
107	EP 649091 A	☒	Correction and modification of microprocessor operations - selectively interfering with instruction flow and control and status signals to correct chip design errors	
108	EP 592121 A	☒	Maintaining translation lookaside buffer coherency - using memory management unit and associated translation lookaside buffers for translating effective addresses into real memory addresses	
109	EP 469239 A	☒	Detection and correction appts. for faulty processor operational codes - detects faulty instructions using logic nor circuit and replaces them with error-free micro-code from programmable array	
110	EP 306209 A	☒	Dual rail processors with error checking at single rail interfaces - has shared resource devices coupled to processors for receiving data from output instructions from processors simultaneously	
111	JP 01046578 A	☒	Arc furnace skimmer scraper locus correction process - uses control unit which has device which memories operation route of skimmer scraper	
112	EP 302614 A	☒	Speech recognition system using minimum of instruction signals - analyses speech input by digitising it and comparing it with library of known sounds	
113	US 4761691 A	☒	Controlling video signal time base corrector - using editor which sends schedules of instructions to VTR control system which communicates selected instructions to time base corrector	
114	JP 62288904 A	☒	Remote control system preventing incorrect output - has operating device to select operation and instruct operation and applies double action method NoAbstract Dwg 0/6	
115	IT 1185976 B	☒	Motor vehicle incorrect gear selection electronic alarm - is for e.g. driver instruction NoAbstract	
116	DE 3544378 A	☒	Transmitting information between participants using bus system - selecting and sending instruction from allocation storage to establish valid connection for duration of corresp. bus procedure	
117	FR 2587518 A	☒	Virtual machine system for processing of exception or interrupts - uses control sequence with improved handling of register data to increase speed of virtual machine operation	
118	EP 211384 A	☒	Pre-fetch monitor information processing system - objects instructions which result in execution of corresp. sequencer of instructions using execution queue	

	Document ID	U	Title	Current OR
119	DE 3586234 G	☒	Subroutine for compiling computer programs - controls given operation by instructions of different lengths and determines maximum number of register positions needed for instruction	
120	US 4488228 A	☒	Virtual memory data processor - stores information relating to internal state upon detection of access fault during instruction execution	
121	JP 58182113 A	☒	Signal compensating device in decoding of digital signal - can selectively change instruction signal providing appropriate correction depending on detected burst length. NoAbstract Dwg 0/6	
122	EP 66082 A	☒	Micro-program control store for data processing system - provides micro-code assisted corrective action by substituting erroneous micro-instruction, accessed from read only store, with another	
123	SU 903939 B	☐	Teaching equipment based on answer selection by student - has displays for incorrect answer analyses controlled by instructor to avoid waste of instructor time	

	L #	Hits	Search Text	DBs
1	L1	9161	instruction near10 (valid$3 invalid$3 correct incorrect)	USPAT; US-PGPUB
2	L4	418	(instruction near10 (valid$3 invalid$3 correct incorrect)).ab,ti.	USPAT; US-PGPUB
3	L6	34856	instruction near10 (select$3 replac$5 substitut$3)	USPAT; US-PGPUB
4	L7	694	1 near99 6	USPAT; US-PGPUB
5	L8	87	7 and 4	USPAT; US-PGPUB
6	L9	2570	instruction near10 (valid$3 invalid$3 correct incorrect)	EPO; JPO; DERWENT; IBM_TDB
7	L10	13056	instruction near10 (select$3 replac$5 substitut$3)	EPO; JPO; DERWENT; IBM_TDB
8	L11	123	9 near99 10	EPO; JPO; DERWENT; IBM_TDB

	Document ID	U	Title	Current OR
1	JP 2003076576 A	☐	SEMICONDUCTOR DEVICE	
2	JP 2002335390 A	☒	IMAGE PROCESSING UNIT AND IMAGE PROCESSING METHOD	
3	JP 2001306551 A	☒	METHOD AND DEVICE FOR PREPARING HTML DATA	
4	JP 2000357096 A	☒	METHOD AND DEVICE FOR PROGRAM CONVERSION AND PROGRAM PROVISION MEDIUM	
5	JP 2000347862 A	☒	INSTRUCTION REPLACING CIRCUIT	
6	JP 2000222218 A	☒	COMPILING DEVICE AND RECORD MEDIUM	
7	JP 2000181753 A	☒	FAULT RECOVERY METHOD, FAULT RECOVERY SYSTEM FOR THE SAME AND COMPUTER READABLE PROGRAM RECORDING MEDIUM	
8	JP 2000177808 A	☒	INVENTORY CONTROL COMPUTER SYSTEM AND METHOD	
9	JP 2000076064 A	☒	METHOD AND SYSTEM FOR INSERTING WATERMARK INTO PROGRAM	
10	JP 2000035893 A	☒	METHOD FOR STATICALLY INITIALIZING ARRANGEMENT OF DATA PROCESSING SYSTEM, DATA PROCESSING METHOD, DATA PROCESSING SYSTEM AND COMPUTER READABLE STORAGE MEDIUM STORING PROGRAM MAKING COMPUTER EXECUTE ITS CONTROL PROCEDURE	
11	JP 11345170 A	☒	COMPUTER SYSTEM FOR SHORTENING EXECUTION OF SPECIFIED INSTRUCTION ON CACHE MEMORY	
12	JP 11306019 A	☒	INFORMATION PROCESSING DEVICE AND PROCESSOR	
13	JP 11265345 A	☒	PROGRAM EXECUTION MANAGING DEVICE	
14	JP 11143865 A	☒	SYSTEM AND METHOD FOR HTML DOCUMENT GENERATION FOR WWW-OLTP COOPERATION SYSTEM	
15	JP 10340228 A	☒	MICROPROCESSOR	
16	JP 10260565 A	☒	ELECTROPHOTOGRAPHIC IMAGE FORMING DEVICE	
17	JP 10228382 A	☒	COMPILING SYSTEM	
18	JP 10222361 A	☒	ROM PROGRAM MONITOR DEVICE IN PROCESSOR OF COMPUTER OR THE LIKE	
19	JP 10011320 A	☒	ROM PROGRAM MONITOR DEVICE OF PROCESSOR OF COMPUTER OR THE LIKE	

	Document ID	U	Title	Current OR
20	JP 09160768 A	☒	PROGRAM EXECUTION DEVICE	
21	JP 09138847 A	☒	PICTURE PROCESSING METHOD/DEVICE	
22	JP 09044351 A	☒	METHOD AND PROCESSOR FOR CHANGING PROGRAM	
23	JP 08235138 A	☒	COMPUTER SYSTEM	
24	JP 08147192 A	☒	DIGITAL SIGNAL PROCESSOR	
25	JP 08006228 A	☒	PIXEL SCRAMBLE IMAGE PROCESSING DEVICE	
26	JP 07152762 A	☒	DOCUMENT PROCESSING METHOD	
27	JP 07044419 A	☒	MICROCOMPUTER DEVELOPMENT BACK UP DEVICE	
28	JP 07036677 A	☒	LINKAGE EDITOR	
29	JP 05257931 A	☒	SENTENCE EDITOR	
30	JP 05233359 A	☒	DEBUGGING DEVICE	
31	JP 05061668 A	☒	MICROCOMPUTER	
32	JP 04367029 A	☒	PROGRAMMING DEVICE FOR PROGRAMMABLE CONTROLLER	
33	JP 04291616 A	☒	ADDITIONAL OPERATION EXECUTION SYSTEM FOR EXTERNAL STORAGE DEVICE	
34	JP 04287135 A	☒	PROCESSOR FOR ELECTRONIC COMPUTER	
35	JP 04225428 A	☒	DATA PROCESSING SYSTEM PROVIDED WITH PERFORMANCE IMPROVING INSTRUCTION CACHE	
36	JP 04111127 A	☒	ARITHMETIC PROCESSOR	
37	JP 04075138 A	☒	PROGRAM SIZE COMPRESSION DEVICE	
38	JP 04052962 A	☒	ACCESS MASK CONTROL SYSTEM	
39	JP 03256225 A	☒	INFORMATION RECORDING/REPRODUCING DEVICE	
40	JP 03078038 A	☒	IN-CIRCUIT EMULATOR	
41	JP 02308333 A	☒	CODING SYSTEM FOR LOGICAL LANGUAGE	
42	JP 02126565 A	☒	OPERATION STOPPING METHOD FOR FUEL CELL	

	Document ID	U	Title	Current OR
43	JP 02109 133 A	☒	CUSTOMIZING SYSTEM FOR PACKAGE SOFTWARE	
44	JP 02108 135 A	☒	PROGRAM TRACING CONTROL SYSTEM	
45	JP 01147 638 A	☒	INSTRUCTION EXECUTION DETECTOR	
46	JP 01144 129 A	☒	CENTRAL PROCESSING UNIT	
47	JP 01076 243 A	☒	INFORMATION PROCESSOR	
48	JP 01035 637 A	☒	PROGRAM TRACING SYSTEM	
49	JP 63093 050 A	☒	DATA FLOW TRACING DEVICE	
50	JP 63036 334 A	☒	ZONE FORM DECIMAL ADDITION SYSTEM	
51	JP 63036 333 A	☒	ZONE FORM DECIMAL SUBTRACTION SYSTEM	
52	JP 63026 760 A	☒	BUFFER MEMORY DEVICE	
53	JP 63008 851 A	☒	CACHE MEMORY CONTROL SYSTEM	
54	JP 62219 073 A	☒	GRAPHIC DATA RESTORATION SYSTEM IN GRAPHIC PROCESSING SYSTEM	
55	JP 62097 450 A	☒	TRANSMISSION CONTROL SYSTEM IN COMMUNICATION FAILURE TIME	
56	JP 62050 912 A	☒	WORK ASSIGNING CONTROL SYSTEM TO UNMANNED TRANSPORTING VEHICLE	
57	JP 61013 329 A	☒	ELECTRONIC APPARATUS	
58	JP 60237 568 A	☒	DATA PROCESSING SYSTEM	
59	JP 60217 037 A	☒	METHOD OF CONTROLLING TOOL STORAGE MAGAZINE AND ITS DEVICE	
60	JP 60007 536 A	☒	INFORMATION PROCESSOR	
61	JP 58159 284 A	☒	BUFFER MEMORY CONTROL SYSTEM	
62	JP 58082 304 A	☒	PROGRAMMABLE CONTROLLER	
63	JP 58076 950 A	☒	DIAGNOSTIC SYSTEM FOR PROGRAM	
64	JP 58062 747 A	☒	PROGRAM JOINT EDITING SYSTEM	
65	JP 58056 044 A	☒	PROTECTION SYSTEM FOR RUNAWAY OF INFORMATION PROCESSOR	

	Document ID	U	Title	Current OR
66	JP 58037 732 A	☒	CHARACTER INPUT DEVICE	
67	JP 58016 350 A	☒	MEMORY EXTENSION SUBSTITUTING SYSTEM	
68	JP 58002 946 A	☒	MEMORY EXTENDING SUBSTITUTION SYSTEM	
69	JP 58002 945 A	☒	MEMORY EXTENDING SUBSTITUTION SYSTEM	
70	JP 58002 944 A	☒	MEMORY EXTENDING SUBSTITUTION SYSTEM	
71	JP 58002 943 A	☒	MEMORY EXTENDING SUBSTITUTION SYSTEM	
72	JP 56135 204 A	☒	PROGRAMMABLE CONTROLLER	
73	JP 54083 727 A	☒	MEMORY FAULT RESTORATION SYSTEM	
74	WO 28416 A1	☒	DATA COMPACTION METHOD FOR AN INTERMEDIATE OBJECT CODE PROGRAMME EXECUTABLE IN AN ONBOARD SYSTEM PROVIDED WITH DATA PROCESSING RESOURCES AND CORRESPONDING ONBOARD SYSTEM WITH MULTIPLE APPLICATIONS	
75	EP 89715 6 A1	☒	DEVICE AND METHOD FOR PREPARING ORIGINAL TEXT AND PROGRAM STORING MEDIUM FOR THE SAME	
76	EP 88459 9 A1	☒	Programming mode selection with jtag circuits	
77	WO 98483 53 A1	☒	WRITE BARRIER SYSTEM AND METHOD INCLUDING POINTER-SPECIFIC INSTRUCTION VARIANT REPLACEMENT MECHANISM	
78	WO 98483 51 A1	☒	GENERATION ISOLATION SYSTEM AND METHOD FOR GARBAGE COLLECTION	
79	EP 87431 6 A2	☒	System and method for assisting exact garbage collection by segregating the contents of a stack into sub stacks	
80	WO 98320 81 A1	☒	DEVICE AND METHOD FOR PREPARING ORIGINAL TEXT AND PROGRAM STORING MEDIUM FOR THE SAME	
81	WO 97011 48 A1	☒	POS TERMINAL WITH REPLACEABLE PRINTER CARTRIDGE	
82	EP 60680 3 A1	☒	Method for detecting program execution errors.	
83	EP 13588 8 A2	☒	Process for preventing the execution of a programme in a computer which is not allowed to execute said programme	
84	NN720 91248	☒	Dynamic Patch Via Invalid Operations. September 1972.	
85	NN710 22543	☒	System Map. February 1971.	
86	US 20030 08443 2 A	☒	Intermediate code preprocessing apparatus for mobile telephone, substitutes specified instruction pattern included in Java class file, with alternative instruction	
87	US 20030 06747 3 A	☒	Predefined code set execution method for programmable vertex shader, involves executing specified substitute instructions using intermediate result obtained by executing another instruction using not more than n input operands	

	Document ID	U	Title	Current OR
88	JP 2003031456 A	☒	Semiconductor fabrication machine evaluation program has instructions for substituting time consumed by machine, in specific equation, to predict performance of machine	
89	US 20020198828 A	☒	Invoice presentment/bill payment system for e-commerce applications, has modular business object that is replaced with another modular object using global information related to biller and payer systems	
90	US 20020198798 A	☒	Modular business transaction platform for e-commerce application, has application server that permits replacement of business object with another business object with specific instructions using same global information	
91	US 20020147902 A	☒	Load operation execution method in processor system, involves associating conditional operator specifying load behavior, with conditional fault instruction to determine whether to retain or replace accessed data	
92	JP 2002304858 A	☒	Digital variable frequency oscillator apparatus for floppy disk drive, corrects synchronous counter of one of VFO circuit by substituting counter value of circuit selected based on peak shift of input data	
93	US 6457118 B	☒	Instruction checking performance method for computer system, involves detecting dependencies between operands in instruction and operands in subsequent instruction in pipeline using source operand	
94	JP 2002218219 A	☒	Portrait photography digital image processing system has image editor to perform automatic synthesis of digitized portrait image photograph by camera with substitute image	
95	US 20020085186 A	☒	Image forming apparatus executes print instruction by changing size of recording medium, to size of substitute recording medium	
96	JP 2002163107 A	☒	Automatic program production apparatus in large scale plants, replaces attribute information if specific character row is contained in instruction	
97	US 6401195 B	☒	Processor pipeline control method for computer system, involves stalling pipeline after detecting hazard in register and storing stale data of register in operand latch of executing stage of pipeline	
98	US 6388585 B	☒	Data decompression program includes decompression instruction to include specified number of addition characters at specific intervals between characters which are shifted current position to another position	
99	US 20020002440 A	☒	Loop diagnosis system for disk array apparatus, suspends execution of any instruction in specific loop of recording unit when loop abnormality is monitored, and substitutes other loop for further instruction execution	
100	US 6408382 B	☒	Application specific program generation involves converting native program by replacing set of native instructions with abbreviated instruction set determined by processing debugged native program	
101	WO 2001204530 A	☒	Modification of control store executable micro instructions for correction of programming errors stored in ROM, where a generated interrupt triggers a jump from ROM to compare and substitute the stored subroutine in RAM	
102	WO 2000284160 A	☒	Method for data compaction of intermediate object code executable in an on board system, comprises substitution of frequently occurring identical sequences in code by specific operating code	
103	US 6058456 A	☒	Cache architecture for computer system, has cache replacement mechanism to restrict replacement of evicted cache block to specific instruction and data classes of values, based on desired cache usage ratio	
104	CN 1243284 A	☒	Method for converting super medium document into speech sound	
105	US 5940872 A	☒	Virtual to physical memory translation storage method in a translation look aside buffer	

	Document ID	U	Title	Current OR
106	EP 884678 A	☒	Call instruction replacement method in computer - checks and determines capability of target computer to execute instruction in program to be loaded into computer; if so retrieves address specifying call location instruction to be replaced and carries out replacement	
107	US 5891182 A	☒	Bio=active frequency generator - uses replaceable control memories to instruct frequency synthesizer to generate specific precise frequencies depending on particular application	
108	US 5953736 A	☒	Write barrier apparatus e.g. for isolating generations in garbage collectors - has non quick to quick translator cache providing pointer specific store instruction replacement with self modifying code provides pointer specific stores instruction replacement	
109	JP 10228382 A	☒	Compile system for converting high class program to target program - has non-aryne access processing unit converts section of non-aryne access by combining with logical operation instruction, aryne access instruction and shift instruction	
110	JP 10222361 A	☒	ROM program monitor in computer - replaces instruction in memory with instruction stored in resource or instruction register, when memory instruction is in accord with instruction stored in resource register	
111	WO 9832081 A	☒	Text preparing device with program storage medium - uses parameter setting table with compiler for preparing original text by sticking specific character in accordance with instruction from substitute detection key	
112	JP 10011320 A	☒	Monitoring apparatus e.g. for program stored in ROM of computers - has instruction registration unit in which specific instructions stored in memory are replaced corresponding to device chosen by device selection flag based on predetermined condition	
113	JP 09198337 A	☒	Processing equipment e.g. computer - replaces instruction stored by memory with instruction corresponding to device designated as object of monitor when stored instruction agrees with specific instruction stored by registration buffer	
114	JP 09185525 A	☒	Protocol debugging method used in ROM program execution in computer - involves making controller to execute protocol debug and replace processing equipment in executing specific instruction based on comparison between instruction and registered specific instruction	
115	JP 09160768 A	☒	Program execution device for computer - has address transformation unit which outputs second address signal to RAM if address of instruction designated is in accord with address of specific instruction in memory area	
116	US 5634118 A	☒	Processor for instructions particularly in execution of stack-position exchange instruction in stack-base architecture - uses exchange instruction for exchanging contents of exchange-destination register with contents of exchange-source register	
117	TW 258805 A	☒	Instructions sorter for multi-processor computing system - excludes ineffective instruction, i.e. such that has nothing to do with master or slave processor in which sorter is installed	
118	EP 606803 A	☒	Error detection procedure for run-time errors in computer control system - using encoding of inputs to replicated blocks and inverse decoding before comparing outputs of blocks	
119	US 5113370 A	☒	Instruction buffer control system for information processor - allocates part of instructions into specified area of buffer which are not replaced during execution of loop of instruction	
120	EP 354031 A	☒	Graphical image editing method for CAD - substituting user-specified replacements for graphical properties found of pattern matches	
121	EP 288760 A	☒	Data processor for re-executing instructions - executes correctly access to I=O address after re-execution following of page replacement after page fault	

	Document ID	U	Title	Current OR
122	EP 250702 A	☒	Cache memory method with variable fetch and replacement schemes - having cache control indicating type of data structure included in memory and selecting appropriate replacement scheme for block swapping	
123	CA 1229928 A	☒	Non-iterative processor for iterative functions in data processing - has ALU using high speed barrel shifter to write over N-value specified in program for actual value of variable	
124	US 4682513 A	☒	Repair kit for detent cables - has repair component snapped in place with sealant between it and remainder of cable	
125	EP 205332 A	☒	Colour modification in image reproduction system - has digital colour component signals for each pixel applied to look up tables producing operation number signal	
126	EP 113398 A	☒	Indexed-indirect addressing method using prefix codes in DP - fetching prefix code in instruction stream and fetching word in main memory at address specified by index register	
127	DE 3334579 A	☒	Encachement appts. for digital computer system - has two cache(s) whose outputs selected by multiplexers are combined in adder	
128	EP 66084 A	☒	Micro-instruction substituting device for dat processor - provides corrective action in control store for faulty instruction read from store of data processor to control store	
129	NL 7507532 A	☒	Program controlled information carrier - in which special instruction words selectively replace instruction words	
130	DE 2356200 A	☒	Data processing system for indexing and substitution of addresses - operates on a single instruction specifying index registers	
131	GB 1391701 A	☐	Time sharing digital computer system - allowing relocation of user programs in memory using base relative addressing system	

	Document ID	U	Title	Current OR
1	US 20030142872 A1	☐	Image processing apparatus, decoding device, encoding device, image processing system, image processing method, and encoding method	382/236
2	US 20030135779 A1	☒	Microprocessor	713/600
3	US 20030135778 A1	☒	Data processing system	713/600
4	US 20030101333 A1	☒	Data processor	712/226
5	US 20030056080 A1	☒	Register read circuit using the remainders of modulo of a register number by the number of register sub-banks	711/219
6	US 20030035486 A1	☒	MPEG encoding apparatus, MPEG decoding apparatus, and encoding program	375/240.26
7	US 20030031467 A1	☒	Data structure of stream data, and recording and playback method thereof	386/95
8	US 20030028754 A1	☒	Data processor using indirect register addressing	712/209
9	US 20030005011 A1	☒	Sticky z bit	708/490
10	US 20020199081 A1	☒	Data processing system and control method	712/34
11	US 20020193893 A1	☒	Data processing device with an indexed immediate addressing mode	700/94
12	US 20020184472 A1	☒	Microcomputer	712/33
13	US 20020174321 A1	☒	System, method and apparatus for allocating hardware resources using pseudorandom sequences	712/218
14	US 20020147902 A1	☒	Method for encoding an instruction set with a load with conditional fault instruction	712/244
15	US 20020133784 A1	☒	Automatic design of VLIW processors	716/1
16	US 20020129227 A1	☒	Processor having priority changing function according to threads	712/228
17	US 20020124216 A1	☒	Integrated circuit and method of operation of such a circuit	714/726

	Document ID	U	Title	Current OR
18	US 20020124044 A1	☒	Method of handling branching instructions within a processor, in particular a processor for digital signal processing, and corresponding processor	709/200
19	US 20020120914 A1	☒	Automatic design of VLIW processors	716/17
20	US 20020114182 A1	☒	Write state machine architecture for flash memory internal instructions	365/185.01
21	US 20020087846 A1	☒	Reconfigurable processing system and method	712/229
22	US 20020075746 A1	☒	Fast accessible dynamic type semiconductor memory device	365/230.03
23	US 20020073262 A1	☒	Pre-stored vector interrupt handling system and method	710/260
24	US 20020062436 A1	☒	METHOD FOR PROVIDING EXTENDED PRECISION IN SIMD VECTOR ARITHMETIC OPERATIONS	712/210
25	US 20020057889 A1	☒	Recording method of stream data and data structure thereof	386/1
26	US 20020057888 A1	☒	Recording method of stream data and data structure thereof	386/1
27	US 20020057887 A1	☒	Recording method of stream data and data structure thereof	386/1
28	US 20020057886 A1	☒	Recording method of stream data and data structure thereof	386/1
29	US 20020039480 A1	☒	Recording medium of stream data, and recording method and playback method of the same	386/68
30	US 20020024892 A1	☒	Recording medium of stream data, and recording method and playback method of the same	369/30.25
31	US 20020012528 A1	☒	Recording method of stream data and data structure thereof	386/95
32	US 20010034828 A1	☒	MICROCODE SCALABLE PROCESSOR	712/245
33	US 20010032304 A1	☒	Processor for making more efficient use of idling components and program conversion apparatus for the same	712/24
34	US 20010012438 A1	☒	Recording method of stream data and data structure thereof	386/65

	Document ID	U	Title	Current OR
35	US 20010010754 A1	☒	Recording method of stream data and data structure thereof	386/65
36	US 20010010753 A1	☒	Recording method of stream data and data structure thereof	386/65
37	US 20010010752 A1	☒	Recording method of stream data and data structure thereof	386/65
38	US 20010010671 A1	☒	Recording medium of stream data, and recording method and playback method of the same	369/47.28
39	US 20010010664 A1	☒	Recording medium of stream data, and recording method and playback method of the same	369/30.1
40	US 20010010642 A1	☒	Static random access memory (SRAM) array central global decoder system and method	365/154
41	US 20010008498 A1	☒	Fast accessible dynamic type semiconductor memory device	365/230.03
42	US 6631463 B1	☒	Method and apparatus for patching problematic instructions in a microprocessor using software interrupts	712/227
43	US 6618291 B2	☒	Write state machine architecture for flash memory internal instructions	365/185.29
44	US 6604193 B1	☒	Processor in which register number translation is carried out	712/228
45	US 6597595 B1	☒	Content addressable memory with error detection signaling	365/49
46	US 6593973 B1	☒	Method and apparatus for providing information in video transitions	348/584
47	US 6587392 B2	☒	Fast accessible dynamic type semiconductor memory device	365/230.03
48	US 6581187 B2	☒	Automatic design of VLIW processors	716/1
49	US 6581129 B1	☒	Intelligent PCI/PCI-X host bridge	710/306
50	US 6580869 B1	☒	Recording medium of stream data including management information used to access the stream data, and recording method and playback method of the same	386/68
51	US 6539470 B1	☒	Instruction decode unit producing instruction operand information in the order in which the operands are identified, and systems including same	712/208
52	US 6522705 B1	☒	Processor for digital data	375/341
53	US 6505292 B1	☒	Processor including efficient fetch mechanism for L0 and L1 caches	712/207
54	US 6490716 B1	☒	Automated design of processor instruction units	716/18

	Document ID	U	Title	Current OR
55	US 6487629 B1	☒	Semiconductor memory for operation in a plurality of operational modes	711/104
56	US 6477632 B1	☒	Storage device and accessing method	711/203
57	US 6457117 B1	☒	Processor configured to predecode relative control transfer instructions and replace displacements therein with a target address	712/213
58	US 6456783 B1	☒	Data structure of stream data, and recording and playback method thereof	386/125
59	US 6453116 B1	☒	Recording medium of stream data, and recording method and playback method of the same	386/68
60	US 6442514 B1	☒	Method and system for simulating a communications bus	703/21
61	US 6438676 B1	☒	Distance controlled concatenation of selected portions of elements of packed data	712/22
62	US 6434690 B1	☒	Microprocessor having a DSP and a CPU and a decoder discriminating between DSP-type instructions and CUP-type instructions	712/35
63	US 6424989 B1	☒	Object-oriented transaction computing system	709/201
64	US 6412067 B1	☒	Backing out of a processor architectural state	712/245
65	US 6408428 B1	☒	Automated design of processor systems using feedback from internal measurements of candidate systems	716/17
66	US 6405302 B1	☒	Microcomputer	712/35
67	US 6385757 B1	☒	Auto design of VLIW processors	716/1
68	US 6381191 B2	☒	Fast accessible dynamic type semiconductor memory device	365/230.03
69	US 6367001 B1	☒	Processor including efficient fetch mechanism for L0 and L1 caches	712/205
70	US 6366526 B2	☒	Static random access memory (SRAM) array central global decoder system and method	365/230.06
71	US 6363408 B1	☒	Method and apparatus for summing selected bits from a plurality of machine vectors	708/670
72	US 6360312 B1	☒	Processor for making more efficient use of idling components and program conversion apparatus for the same	712/215
73	US 6356995 B2	☒	Microcode scalable processor	712/209
74	US 6351806 B1	☒	Risc processor using register codes for expanded instruction set	712/225
75	US 6349297 B1	☒	Information processing system for directing information request from a particular user/application, and searching/forwarding/retrieving information from unknown and large number of information resources	707/4
76	US 6339424 B1	☒	Drawing processor	345/419

	Document ID	U	Title	Current OR
77	US 6334184 B1	☒	Processor and method of fetching an instruction that select one of a plurality of decoded fetch addresses generated in parallel to form a memory request	712/235
78	US 6314443 B1	☒	Double/saturate/add/saturate and double/saturate/subtract/saturate operations in a data processing system	708/552
79	US 6308261 B1	☒	Computer system having an instruction for probing memory latency	712/219
80	US 6272615 B1	☒	Data processing device with an indexed immediate addressing mode	711/220
81	US 6269436 B1	☒	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
82	US 6253307 B1	☒	Data processing device with mask and status bits for selecting a set of status conditions	712/209
83	US 6233590 B1	☒	Server apparatus for distributed communications supporting multiple user/application environment	715/500
84	US 6212236 B1	☒	Image decoding apparatus	375/240.12
85	US 6199154 B1	☒	Selecting cache to fetch in multi-level cache system based on fetch address source and pre-fetching additional data to the cache for future access	712/205
86	US 6189092 B1	☒	Pipeline processor capable of reducing branch hazards with small-scale circuit	712/241
87	US 6189068 B1	☒	Superscalar microprocessor employing a data cache capable of performing store accesses in a single clock cycle	711/3
88	US 6185670 B1	☒	System for reducing number of opcodes required in a processor using an instruction format including operation class code and operation selector code fields	712/208
89	US 6178492 B1	☒	Data processor capable of executing two instructions having operand interference at high speed in parallel	712/23
90	US 6175532 B1	☒	Fast accessible dynamic type semiconductor memory device	365/230.03
91	US 6170998 B1	☒	Processor which returns from a subroutine at high speed and a program translating apparatus which generates machine programs that makes a high-speed return from a subroutine	717/154
92	US 6170052 B1	☒	Method and apparatus for implementing predicated sequences in a processor with renaming	712/236
93	US 6167509 A	☒	Branch performance in high speed processor	712/237
94	US 6167506 A	☒	Replacing displacement in control transfer instruction with encoding indicative of target address, including offset and target cache line location	712/213
95	US 6151598 A	☒	Digital dictionary with a communication system for the creating, updating, editing, storing, maintaining, referencing, and managing the digital dictionary	707/3
96	US 6134649 A	☒	Control transfer indication in predecode which identifies control transfer instruction and an alternate feature of an instruction	712/204
97	US 6125440 A	☒	Storing executing instruction sequence for re-execution upon backward branch to reduce power consuming memory fetch	712/205
98	US 6115757 A	☒	DMA control apparatus for multi-byte serial-bit transfer in a predetermined byte pattern and between memories associated with different asynchronously operating processors for a distributed system	710/22

	Document ID	U	Title	Current OR
99	US 6112289 A	☒	Data processor	712/23
100	US 6105125 A	☒	High speed, scalable microcode based instruction decoder for processors using split microROM access, dynamic generic microinstructions, and microcode with predecoded instruction information	712/209
101	US 6101596 A	☒	Information processor for performing processing without register conflicts	712/216
102	US 6092183 A	☒	Data processor for processing a complex instruction by dividing it into executing units	712/215
103	US 6079039 A	☒	Test circuit and test method for testing semiconductor chip	714/726
104	US 6076158 A	☒	Branch prediction in high-performance processor	712/230
105	US 6076155 A	☒	Shared register architecture for a dual-instruction-set CPU to facilitate data exchange between the instruction sets	712/225
106	US 6075527 A	☒	Interactive television system	345/721
107	US 6061786 A	☒	Processor configured to select a next fetch address by partially decoding a byte of a control transfer instruction	712/237
108	US 6058255 A	☒	JTAG instruction decode test register and method	716/4
109	US 6055652 A	☒	Multiple segment register use with different operand size	714/53
110	US 6049897 A	☒	Multiple segment register use with different operand size	714/53
111	US 6049862 A	☒	Signal processor executing compressed instructions that are decoded using either a programmable or hardwired decoder based on a category bit in the instruction	712/208
112	US 6044460 A	☒	System and method for PC-relative address generation in a microprocessor with a pipeline architecture	712/244
113	US 6028810 A	☒	Fast accessible dynamic type semiconductor memory device	365/230.03
114	US 6026485 A	☒	Instruction folding for a stack-based machine	712/226
115	US 6023759 A	☒	System for observing internal processor events utilizing a pipeline data path to pipeline internally generated signals representative of the event	712/227
116	US 6014734 A	☒	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
117	US 6009203 A	☒	Method and apparatus for hybrid VLC bitstream decoding	382/233
118	US 6006322 A	☒	Arithmetic logic unit and microprocessor capable of effectively executing processing for specific application	712/200
119	US 5995746 A	☒	Byte-compare operation for high-performance processor	712/220
120	US 5991869 A	☒	Superscalar microprocessor including a high speed instruction alignment unit	712/204

	Document ID	U	Title	Current OR
121	US 5987561 A	☒	Superscalar microprocessor employing a data cache capable of performing store accesses in a single clock cycle	711/3
122	US 5987495 A	☒	Method and apparatus for fully restoring a program context following an interrupt	709/108
123	US 5983335 A	☒	Computer system having organization for multiple condition code setting and for testing instruction out-of-order	712/23
124	US 5983004 A	☒	Computer, memory, telephone, communications, and transportation system and methods	709/227
125	US 5978907 A	☒	Delayed update register for an array	712/239
126	US 5966530 A	☒	Structure and method for instruction boundary machine state restoration	712/244
127	US 5938759 A	☒	Processor instruction control mechanism capable of decoding register instructions and immediate instructions with simple configuration	712/209
128	US 5935239 A	☒	Parallel mask decoder and method for generating said mask	712/224
129	US 5933618 A	☒	Speculative register storage for storing speculative results corresponding to register updated by a plurality of concurrently recorded instruction	712/217
130	US 5922068 A	☒	Information processing system and information processing method for executing instructions in parallel	712/215
131	US 5918045 A	☒	Data processor and data processing system	712/237
132	US 5909206 A	☒	Display control device	345/98
133	US 5903262 A	☒	Interactive television system with script interpreter	725/136
134	US 5901300 A	☒	Control store address stop	712/200
135	US 5895486 A	☒	Method and system for selectively invalidating cache lines during multiple word store operations for memory coherence	711/121
136	US 5894548 A	☒	Semiconductor device having test circuit	714/30
137	US 5892936 A	☒	Speculative register file for storing speculative register states and removing dependencies between instructions utilizing the register	712/216
138	US 5890009 A	☒	VLIW architecture and method for expanding a parcel	712/24
139	US 5889982 A	☒	Method and apparatus for generating event handler vectors based on both operating mode and event type	712/229
140	US 5887243 A	☒	Signal processing apparatus and methods	725/136
141	US 5881308 A	☒	Computer organization for multiple and out-of-order execution of condition code testing and setting instructions out-of-order	712/23
142	US 5881278 A	☒	Return address prediction system which adjusts the contents of return stack storage to enable continued prediction after a mispredicted branch	712/242
143	US 5878255 A	☒	Update unit for providing a delayed update to a branch prediction array	712/240

	Document ID	U	Title	Current OR
144	US 5875324 A	☒	Superscalar microprocessor which delays update of branch prediction information in response to branch misprediction until a subsequent idle clock	712/238
145	US 5872948 A	☒	Processor and method for out-of-order execution of instructions based upon an instruction parameter	712/214
146	US 5867726 A	☒	Microcomputer	712/32
147	US 5867712 A	☒	Single chip integrated circuit system architecture for document instruction set computing	717/127
148	US 5867696 A	☒	Saving a program counter value as the return address in an arbitrary general purpose register	712/233
149	US 5864707 A	☒	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
150	US 5864703 A	☒	Method for providing extended precision in SIMD vector arithmetic operations	712/22
151	US 5860104 A	☒	Data cache which speculatively updates a predicted data cache storage location with store data and subsequently corrects mispredicted updates	711/137
152	US 5859992 A	☒	Instruction alignment using a dispatch list and a latch list	712/204
153	US 5854939 A	☒	Eight-bit microcontroller having a risc architecture	712/41
154	US 5852729 A	☒	Code segment replacement apparatus and real time signal processor using same	712/225
155	US 5844828 A	☒	Shift circuit and system having the same	708/209
156	US 5835436 A	☒	Dynamic type semiconductor memory device capable of transferring data between array blocks at high speed	365/230.03
157	US 5832289 A	☒	System for estimating worst time duration required to execute procedure calls and looking ahead/preparing for the next stack operation of the forthcoming procedure calls	712/30
158	US 5832288 A	☒	Element-select mechanism for a vector processor	712/5
159	US 5826071 A	☒	Parallel mask decoder and method for generating said mask	712/224
160	US 5822559 A	☒	Apparatus and method for aligning variable byte-length instructions to a plurality of issue positions	712/214
161	US 5819059 A	☒	Predecode unit adapted for variable byte-length instruction set processors and method of operating the same	712/213
162	US 5812836 A	☒	System for processing iterative tasks in data processing systems	712/220
163	US 5809272 A	☒	Early instruction-length pre-decode of variable-length instructions in a superscalar processor	712/210
164	US 5806068 A	☒	Document data processor for an object-oriented knowledge management system containing a personal database in communication with a packet processor	707/103R
165	US 5805918 A	☒	Dual-instruction-set CPU having shared register for storing data before switching to the alternate instruction set	712/43
166	US 5784632 A	☒	Parallel diagonal-fold array processor	712/11

	Document ID	U	Title	Current OR
167	US 5781789 A	☐	Superscaler microprocessor employing a parallel mask decoder	712/23
168	US 5778423 A	☐	Prefetch instruction for improving performance in reduced instruction set processor	711/118
169	US 5778246 A	☐	Method and apparatus for efficient propagation of attribute bits in an instruction decode pipeline	712/23
170	US 5758114 A	☐	High speed instruction alignment unit for aligning variable byte-length instructions according to predecode information in a superscalar microprocessor	712/204
171	US 5757353 A	☐	Display control device	345/685
172	US 5754766 A	☐	Integrated circuit system for direct document execution	709/200
173	US 5752069 A	☐	Superscalar microprocessor employing away prediction structure	712/23
174	US 5751985 A	☐	Processor structure and method for tracking instruction status to maintain precise state	712/218
175	US 5745758 A	☐	System for regulating multicomputer data transfer by allocating time slot to designated processing task according to communication bandwidth capabilities and modifying time slots when bandwidth change	709/102
176	US 5740418 A	☐	Pipelined processor carrying out branch prediction by BTB	712/239
177	US 5740392 A	☐	Method and apparatus for fast decoding of 00H and OFH mapped instructions	712/210
178	US 5724249 A	☐	System and method for power management in self-resetting CMOS circuitry	716/1
179	US 5703658 A	☐	Video decoder/converter with a programmable logic device which is programmed based on the encoding format	348/554
180	US 5696959 A	☐	Memory store from a selected one of a register pair conditional upon the state of a selected status bit	712/245
181	US 5685009 A	☐	Shared floating-point registers and register port-pairing in a dual-architecture CPU	712/23
182	US 5682544 A	☐	Massively parallel diagonal-fold tree array processor	712/16
183	US 5682521 A	☐	Microprocessor control system which selects operating instructions and operands in an order based upon the number of transferred executable operating instructions	712/200
184	US 5673426 A	☐	Processor structure and method for tracking floating-point exceptions	712/244
185	US 5673408 A	☐	Processor structure and method for renamable trap-stack	712/216
186	US 5671382 A	☐	Information processing system and information processing method for executing instructions in parallel	712/215
187	US 5671226 A	☐	Multimedia information processing system	370/474
188	US 5669011 A	☐	Partially decoded instruction cache	712/23

	Document ID	U	Title	Current OR
189	US 5659721 A	☐	Processor structure and method for checkpointing instructions to maintain precise state	712/228
190	US 5657476 A	☐	Signal processor with delay line management logic	711/166
191	US 5655115 A	☐	Processor structure and method for watchpoint of plural simultaneous unresolved branch evaluation	712/239
192	US 5651124 A	☐	Processor structure and method for aggressively scheduling long latency instructions including load/store instructions while maintaining precise state	712/215
193	US 5649136 A	☐	Processor structure and method for maintaining and restoring precise state at any instruction boundary	712/244
194	US 5644742 A	☐	Processor structure and method for a time-out checkpoint	712/244
195	US 5638525 A	☐	Processor capable of executing programs that contain RISC and CISC instructions	712/209
196	US 5638524 A	☐	Digital signal processor and method for executing DSP and RISC class instructions defining identical data processing or data transfer operations	712/221
197	US 5634136 A	☐	Data processor and method of controlling the same	712/237
198	US 5634118 A	☐	Splitting a floating-point stack-exchange instruction for merging into surrounding instructions by operand translation	712/226
199	US 5630157 A	☐	Computer organization for multiple and out-of-order execution of condition code testing and setting instructions	712/23
200	US 5625840 A	☐	Programmable external storage control apparatus	710/5

DERWENT-ACC-NO: 2001-229019

DERWENT-WEEK: 200325

TITLE: Instruction changing circuit for single-chip microcomputer has selector provided in ROM collection unit having flag of operation which shows implication of selection of correction instruction

---------- KWIC ---------

Standard Title Terms - TTX (1):
INSTRUCTION CHANGE CIRCUIT SINGLE CHIP MICROCOMPUTER SELECT ROM COLLECT UNIT FLAG OPERATE SHOW IMPLICATION SELECT CORRECT INSTRUCTION

PAT-NO: JP408137687A

DOCUMENT-IDENTIFIER: JP 08137687 A

TITLE: PROGRAM CONTROLLER

PUBN-DATE: May 31, 1996

INVENTOR-INFORMATION:
NAME

NO, YOSHIHIRO

KURIYAMA, SEIICHI

ASSIGNEE-INFORMATION:
NAME
COUNTRY
HITACHI LTD
N/A
HITACHI COMPUTER ELECTRON CO LTD
N/A

APPL-NO: JP06276205

APPL-DATE: November 10, 1994

INT-CL (IPC): G06F009/32, G06F009/32

ABSTRACT:

PURPOSE: To improve the processing performance by replacing an instruction of a program with other instruction in the priority processing mode such as high speed processing mode so as to reduce number of program operation steps without executing undesired instructions.

CONSTITUTION: A check circuit 4 checks a valid bit in an instruction designation flag 3 and a priority code flag 1. When valid, an instruction generating circuit 5 generates a skip or branch instruction based on a selection bit in the instruction designation flag 3. A selection circuit 6 selects an instruction generated by the instruction generating circuit 5 and stores the selected instruction to an instruction registration 7. When it is discriminated by the check circuit 4 that the instruction is not valid, the instruction code in the register 2 is selected and stored in the instruction register 7.

PAT-NO: JP404111127A

DOCUMENT-IDENTIFIER: JP 04111127 A

TITLE: ARITHMETIC PROCESSOR

PUBN-DATE: April 13, 1992

INVENTOR-INFORMATION:
NAME

UENO, KIYOJI

ASSIGNEE-INFORMATION:
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TOSHIBA CORP
N/A

APPL-NO: JP02230106

APPL-DATE: August 31, 1990

INT-CL (IPC): G06F009/38, G06F015/16

ABSTRACT:

PURPOSE: To attain the effective supply of

S-9/-29

PAT-NO: JP409044351A

DOCUMENT-IDENTIFIER: JP 09044351 A

TITLE: METHOD AND PROCESSOR FOR CHANGING PROGRAM

PUBN-DATE: February 14, 1997

INVENTOR-INFORMATION:
NAME

KODAMA, HISASHI

ARAKI, TOSHIYUKI

ASSIGNEE-INFORMATION:
NAME
COUNTRY
MATSUSHITA ELECTRIC IND CO LTD
N/A

APPL-NO: JP08128857

APPL-DATE: May 23, 1996

INT-CL (IPC): G06F009/06

PAT-NO: JP410011320A

DOCUMENT-IDENTIFIER: JP 10011320 A

TITLE: ROM PROGRAM MONITOR DEVICE OF PROCESSOR OF COMPUTER OR THE LIKE

PUBN-DATE: January 16, 1998

INVENTOR-INFORMATION:
NAME

KUZUMAKI, EMI

ASSIGNEE-INFORMATION:
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APPL-NO: JP08158401

APPL-DATE: June 19, 1996

INT-CL (IPC): G06F011/28, G06F009/06

ABSTRACT:

PAT-NO: JP02000357096A

DOCUMENT-IDENTIFIER: JP 2000357096 A

TITLE: METHOD AND DEVICE FOR PROGRAM CONVERSION AND PROGRAM PROVISION MEDIUM

PUBN-DATE: December 26, 2000

INVENTOR-INFORMATION:
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FUJINAMI, YORIHISA
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APPL-NO: JP11170058

APPL-DATE: June 16, 1999

INT-CL (IPC): G06F009/45

ABSTRACT: